Paper No. 11

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

***Ex parte*** TAH-KANG J. TING, GYH-BIN WANG, and CHIEN-TE WU

Appeal No. 1999-0853
Application No. 08/709,896

ON BRIEF

Before JERRY SMITH, FLEMING, and RUGGIERO, ***Administrative Patent_Judges***.

FLEMING, ***Administrative Patent Judge***.

## ***DECISION ON APPEAL***

This is a decision on appeal from the final rejection of claims 1 through 17, all the claims pending in the application.

The invention relates to a buffer circuit that includes a Field Effect Transistor (FET) for controlling the hysteresis. The FET (23 or 36) is selected with a desired channel type, phase of its gate signal with respect to the output of the first circuit, and polarity so as to turn on the FET during a

switching transition near the knees of the transfer curve having two parallel paths. See Appellants' specification page 6, line 35 through page 7, line 31. The circuitry arrangement has been chosen such that when the input 18 rises from low to high, no hysteresis occurs and branch 34 is taken whereas when the input transition changes from high to low, hysteresis occurs and branch 33 is taken. See Appellants' Figures 2, 2A and 2B and the specification page 8, line 26 to page 9, line 10.

Independent claim 1 is reproduced as follows:

1. A buffer circuit of the type having a chain of amplifying circuits (**10, 11, 12**) connected output to input between an input pad of a semiconductor chip and circuits that process an input signal at the pad, the chip having two power supply terminals, the chain including a first circuit (**10**) having its output connected to the input of a second amplifying circuit, the second circuit having an input and an output, the transfer curve for the switching operation of the first circuit having high and low substantially constant output levels (**30, 31**) representing binary logic values in response to the input signal and having a steep transition between the high and low output levels and having hysteresis wherein the transition has parallel paths at one knee joining a constant part of the curve to the transition part of the transfer curve, wherein the improvement comprises,

an FET (**23** or **36**) connected to conduct between the output of the first circuit and one of the power supply terminals in response to a gate signal from an output (**15**) of a circuit (**12**) in the chain to form a feedback loop,

the channel type of the FET, the phase of its gate signal with respect to the output of the first circuit, and the polarity of the power supply terminal being selected to turn on the FET during a switching transition near the knee of the transfer curve having the two parallel paths.

## *References*

The references relied on by the Examiner are as follows:

Koyama 4,563,594 Jan. 7, 1986

Shimizu JP 62-155004 Dec. 27, 1988
(Japanese patent)

## *Rejections at Issue*

Claims 1-9 stand rejected under 35 U.S.C. § 102 as being anticipated by Shimizu. Claims 10-17 stand rejected under 35 U.S.C. § 103 as being unpatentable over Shimizu.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the appeal brief[1] and the Answer for the respective details thereof.

[1] Appellants filed an appeal brief on May 14, 1998. On June 19, 1998 the Examiner mailed the Examiner's answer to Appellants.

***OPINION***

After a careful review of the evidence before us, we do not agree with the Examiner that claims 1 through 9 are anticipated by the applied reference.

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. ***See In re King***, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and ***Lindermann Mashinenfabrik GMBH v. American Hoist & Derrick Co.***, 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

Appellants' claim 1 recites the following:

> an FET (23 or 36) connected to conduct between the output of the first circuit and one of the power supply terminals . . .,
>
> the channel type of the FET, the phase of its gate signal with respect to the output of the first circuit, and the polarity of the power supply terminal being selected to turn on the FET during a switching transition near the knee of the transfer curve having the two parallel paths.

Appellants argue on pages 7 and 8 of the brief that neither Shimizu nor Koyama teaches Appellants' claimed limitations as required under 35 U.S.C. § 102. In particular, Appellants argue that the Shimizu and Koyama "references do

not teach or suggest making the feedback connection depend on 'to turn on the FET during a switching transition near the knee of the transfer curve having two parallel paths.'" See page 8, lines 2-6 of the brief.

On page 6, lines 15-17 of the answer, the Examiner argues that Shimizu teaches that "the chain of amplifying circuit is seen as elements 6-8 and under broadest reasonable interpretation, it is clear that the positive feedback (feedback connected from 8 out to 10G) *inherently provides a hysteresis operation recited therein*." Emphasis added. Further, the Examiner argues that, in light of Koyama, showing a conventional Schmitt trigger that also has the transition having parallel paths at one knee joining a constant part of the curve, "[i]t is clear that the applied reference Shimizu with [sic] has the conventional Schmidt [sic, Schmitt] trigger response." See page 6, lines 17-20 and page 7, lines 2 and 3 of the answer. Furthermore, the Examiner argues that "it appears that not only does the Shimizu [reference] show the same structure, but [it] also performs the same function as well." See page 7, lines 10-12 of the answer.

"Anticipation is established only when a single prior art reference discloses, expressly or under principles of inherency, each and every element of a claimed invention." ***RCA Corp. V. Applied Digital Data Sys, Inc.***, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.), cert. dismissed, 468 U.S. 1228 (1984), *citing* ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 772,
218 USPQ 781, 789 (Fed. Cir. 1983). The prior art disclosure need not be expressed in order to anticipate. ***Standard Havens Prods., Inc. V. Gencor Indus., Inc.***, 953 F.2d 1360, 1369, 21 USPQ2d 1321, 1328 (Fed. Cir.) ***cert. denied***, 506 U.S. 817 (1992).

Furthermore, "[t]o establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by person of ordinary skill.'" ***In re Robertson***, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950 (Fed. Cir. 1999) ***citing Continental Can Co. v. Monsanto Co.***, 948 F.3d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991). "Inherency, however, may not be established

by probabilities or possibilities. The mere fact that a certain thing may result for a given set of circumstances is not sufficient." Id. ***citing Continental Can Co. v. Monsanto, Co.***, 948 F.3d 1264, 1269, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991).

Upon careful review of Shimizu, we fail to find that Shimizu teaches:

> an FET (23 or 36) connected to conduct between the output of the first circuit and one of the power supply terminals . . . the channel type of the FET, the phase of its gate signal with respect to the output of the first circuit, and the polarity of the power supply terminal being selected to turn on the FET during a switching transition near the knee of the transfer curve having the two parallel paths

as recited in Appellants' claim 1. Rather, we find that Shimizu illustrates three inverters (6,7 & 8) with $8_{out}$ connected to the gate of 10 via 10G, $6_{out}$ connected to the source of 10 via 10S and power supply 11 connected to the drain of 10 via 10D. See Shimizu Figure 1 and disclosure page 5, line 19 through page 6, line 17. We also find that Shimizu's figures 2 and 3 are disclosed as a prior art circuit and a waveform illustrating the operation of the prior art Schmitt circuit. See page 10, lines 1-3 of Shimizu. We agree

with the Examiner that Shimizu's circuit includes inverters 10, 11 & 12 wherein the output 16 from inverter 10 is connected to the drain 25 of the FET 23, the output 15 from the delay inverters 11 and 12 is connected to the gate 27 and the power supply or ground is connected to the source 26.

However, we cannot look at a limited portion of the circuitry in a vacuum but rather need to analyze the circuit as a whole. We find that Shimizu teaches additional circuitry in which a FET 9 and a ground 12 are connected to the FET 10 via 10S and 10G to compliment the FET 10 (see Shimizu page 6, lines 15-17). This arrangement would certainly affect the operation of FET 10. We are invited by the Examiner to speculate, without further evidence, that the Shimizu FET 10 would inherently provide the same hysteresis operation as claimed by Appellants. We cannot do so.

Further, we find that claims 2 through 8 are dependent on claim 1 and thereby recite the above limitation. Furthermore, we note that claim 9 also includes the above limitation found in claim 1. Therefore, we find that Shimizu fails to teach all of the limitations of claims 1 through 9, and thereby these claims are not anticipated by Shimizu.

On pages 4-6 of the answer, the Examiner argues that claims 10 through 17 are rejected under 35 U.S.C. § 103 as being unpatentable over Shimizu. For the same reasons above, we fail to find that the Examiner has shown that Shimizu teaches or suggests the above claim 9 limitations. Because claims 10 through 17 depend from claim 9, and therefore include all the limitations of claim 9, we will not sustain the Examiner's rejection of claims 10 through 17 under 35 U.S.C. § 103.

In view of the foregoing, the decision of the Examiner rejecting claims 1 through 17 is reversed.

***REVERSED***

JERRY SMITH )

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| Administrative Patent Judge ) | |
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| ) | BOARD OF PATENT |
| MICHAEL R. FLEMING ) | APPEALS |
| Administrative Patent Judge ) | AND |
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| JOSEPH F. RUGGIERO ) | |
| Administrative Patent Judge ) | |

MRF/LBG

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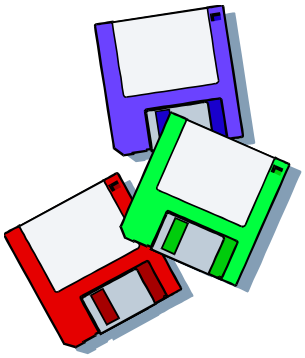

***Lesley***

Appeal No. 1999-0853
Application No. 08/709,869

APJ FLEMING

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DECISION: REVERSED

Prepared: October 8, 2002

Draft Final

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OB/HD GAU

PALM / ACTS 2 / BOOK

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